Update 28/12/2017:

This designed analog/digital switch does not work! And I finally took some time to figure out why.

Input and output have different clock domains in microDSP andloop if only the data is back to input through switch IC2. Does not work as the data is not sync with BCLK and LRCK coming from the SRC.

Unlike original signal naming, input 12S port is slave.

I falsely thought it would work as when you are mastering with microDSP, switching only slave works. But mastering must use the clocks somehow in different way.

I have done a hardware modification where I wire DATOUT5/6 along with OUT_BCLK and OUT_LRCK back to PortB of SRC4392 where they can be routed back here the same way as SPFDIF signal.
DAC output is stated as 6.15 Vpp (differential). Thru, single outputs are ±3 Vpp (±1.5 Vrms), centered at ±2.5 V.

Filter gain = 4 -> differential output = ±6 Vpp = ±3.2 Vrms.

Headroom of OPA662 and PGA4311 with around ±5.3 V supply are sufficient. If component values are to be changed, these considerations must be taken into account.

2nd order Butterworth, MFB, Fc approx 100 kHz.
Microcontroller

Update 28/12/2017:
Some modifications were done for mln05 OLED version so these are marked on here.

OLED used instead of LCD so resistors were removed and G54 signals connected to P13. OLED was then wired to those and supply plus 1–2. The rest of the PORTA pins were used for debugging signals.