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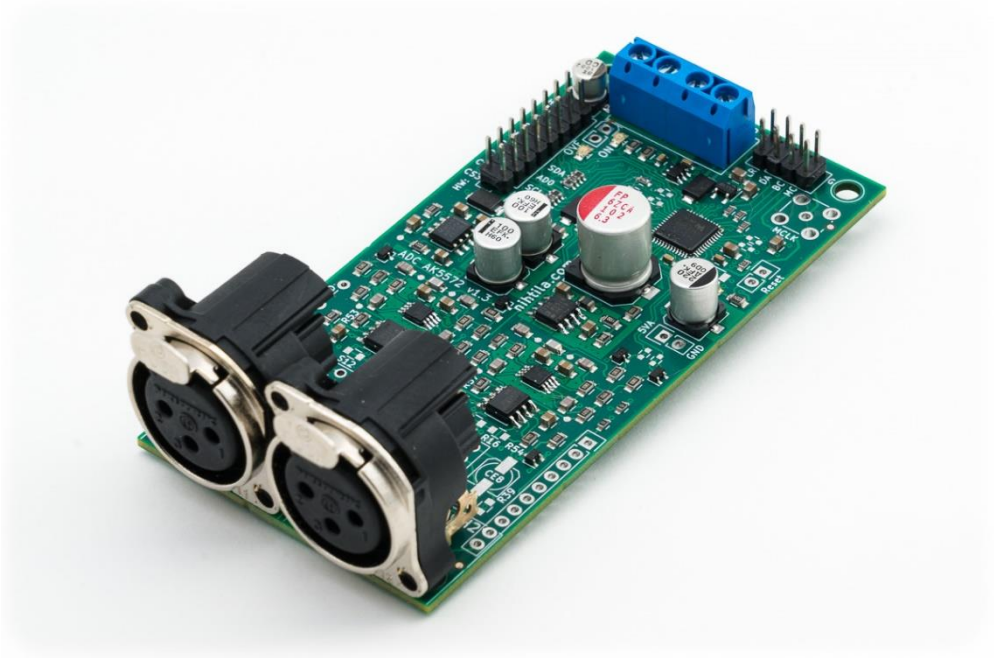
# ADC AK5572 AD-Converter (v1.3)

## Very high performance audio AD-converter



## AUDIO PERFORMANCE

- Up to 768 kHz / 32 bit audio
- 121 dBA dynamic range / SNR
  - 124 dBA in mono mode
- -113 dB THD+N (-1 dBFS, 1 kHz)
- -117 dB THD (-8 dBFS, 1 kHz)
- -130 dB crosstalk (10 kHz)
- 0 dBFS = 4.0 Vrms differential
- Input impedance: 200 kΩ differential, 100 kΩ common mode

*Typical values. Measurement bandwidth is 20 kHz, sample rate 192 kHz, and master clock 24.576 MHz.*

## FEATURES

- Balanced (differential) input
  - XLR connectors
- Stereo or mono operation
- I2S output
  - Master or Slave
  - Flexible clocking options
- HW configurable but supports I2C
- Four digital filter options
- Optional input AC-coupling
- Comprehensive measurement results

## APPLICATIONS

- High performance ADC in Hifi system
- Sound and music recording
- Audio measurement instrument

ADC AK5572 is a very high performance audio AD-converter suitable for sound recording applications or high end audio setups. Alternatively, using this ADC in a DIY audio analyser system one can build a very capable setup when paired with a suitable PC software.

Audio performance is high enough not to be ashamed beside any AD-converter. The board is not very picky in terms of power supply but it must be relatively clean to obtain the high performance figures.

Flexible configuration options are provided by simple jumper links. Remaining configuration bits are accessible with 0 Ω resistors. I2C access can be enabled for programming with Arduino or similar.

There is an LED for power and overflow which flashes if input clips.

Basic input protection with diode clamps is provided. More robust protection is recommended for measurement instrument applications.

Input circuit can be configured as instrumentation amplifier along with optional trimmer on bottom side of PCB for input gain adjustment.

Input connections:

- XLR with max. 4.0 Vrms input signal (in default gain configuration)

Output connections:

- MCLK – Master clock, 24.576 MHz recommended (input)
- LRCK – Word clock (input / output)
- BCLK – Bit clock (input / output)
- DATA – Audio data (output)

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## HARDWARE DETAILS

- AKM AK5572 ADC
- OPA1632 differential opamps
- LM4562 buffers
- 4-layer PCB
- C0G caps in signal path
  - Optional elco for AC-coupling
- Thin film 0.5 % resistors in signal path
- Low noise and low distortion design
- SMB and 50 Ω termination option for Master Clock input
- Design and performance evaluated by comprehensive measurements

## SYSTEM REQUIREMENTS

- 24.576 MHz Master Clock
- Master or Slave I2S input device
- 3.3 V logic level
- Three supplies:
  - 5 V digital, 15 mA
  - +15 V analog, 95 mA
  - -15 V analog, 60 mA
- Decent (passive) cooling; gets warm

## INFORMATION AND CONTACT

- http://nihtila.com for general up to date information and shop
- Youtube for videos
- Follow Twitter (@nihtilacom)
- Contact (http://nihtila.com/contact/)

## DOCUMENT VERSION

v1.3.0 (12/2020) for board v1.3

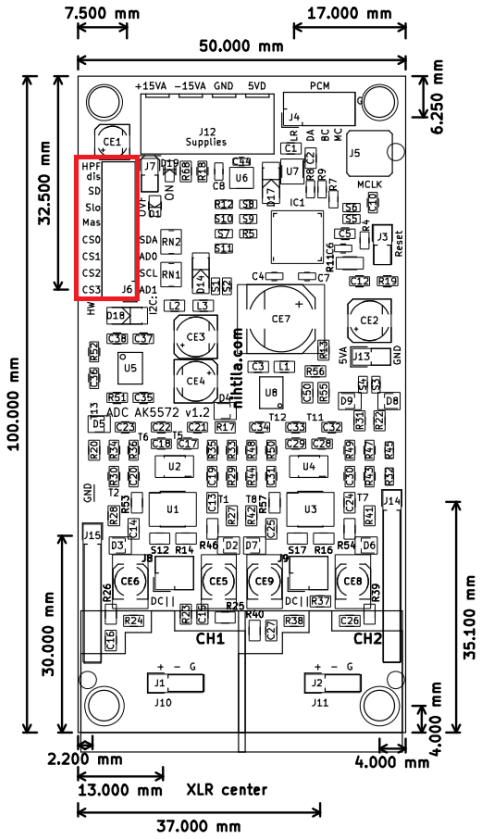
# Configuration and settings

By default jumper header J6 is not populated. Default settings are I2S Slave, auto clock setup, HPF enabled, and Sharp digital filter response. By populating J6 these can be changed.

Jumpers CS0-CS3 configure clocks. See full table in AK5572 datasheet and summary table below. Sample rate depends on MCLK; 24.576 MHz is recommended and also assumed here.

There are four digital low-pass filter options selectable by two jumper links. More details on these filters are on nihtila.com and AK5572 datasheet.

Power toggle or reset is recommended after changing any settings.




By default inputs are DC coupled. Optional AC-coupling capacitors can be populated. When populated, these caps can be shorted with J8/J9.

AC-coupling is normally not needed as there is an internal digital high-pass filter to remove offset caused by input circuit and the ADC IC itself. It is recommended to keep this HPF enabled.

Master clock (MCLK) can be brought to PCM pinheader J4, or optional SMB connector J5 and 50 Ω resistor R11 can be populated.

ADC can be set to I2C mode by changing configuration resistors. Then CS0-CS3 pins become I2C signals. Instructions are on PCB bottom side.

Digital low-pass filter selection on J6.

| SD | Slo | Filter roll-off type |
|---|---|---|
| open | open | Sharp (default) |
| open | close | Slow |
| close | open | Short Delay Sharp |
| close | close | Short Delay Slow |

Sample rate when I2S Master and 24.576 MHz MCLK. **When I2S Slave, keep all open for Auto**.

| CS3 | CS2 | CS1 | CS0 | Sample rate |
|---|---|---|---|---|
| open | close | close | open | 768 kHz |
| open | close | close | close | 384 kHz |
| close | close | close | close | 192 kHz |
| close | close | open | open | 96 kHz |
| close | open | open | close | 48 kHz |

Other jumper links (default in **bold**)

| Jumper | Open | Close |
|---|---|---|
| HPF | **Digital HPF enabled** | HPF disabled |
| Sla | **ADC is I2S Slave** | I2S Master |