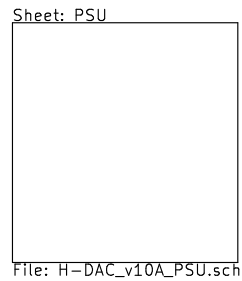
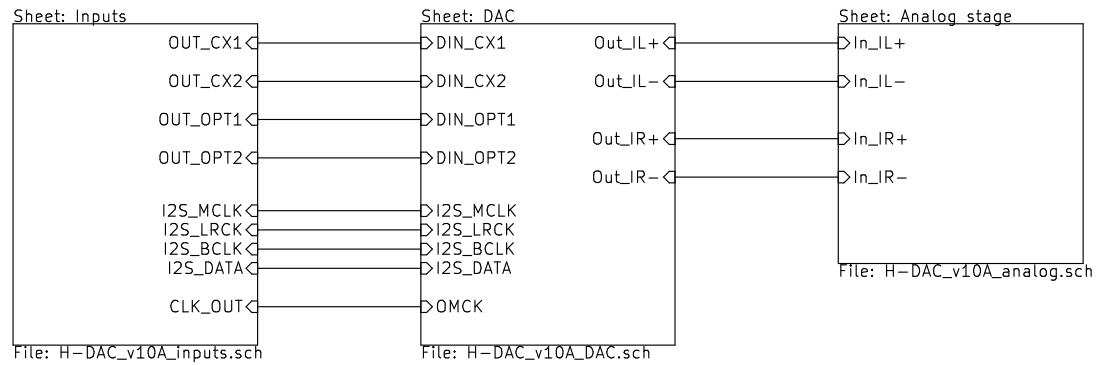


# H-DAC v1.0A

## Root Sheet



**Tomi Nihtilä**

Sheet: /  
File: H-DAC\_v10A.sch

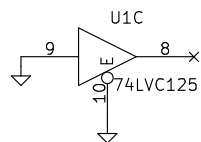
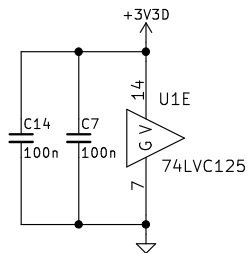
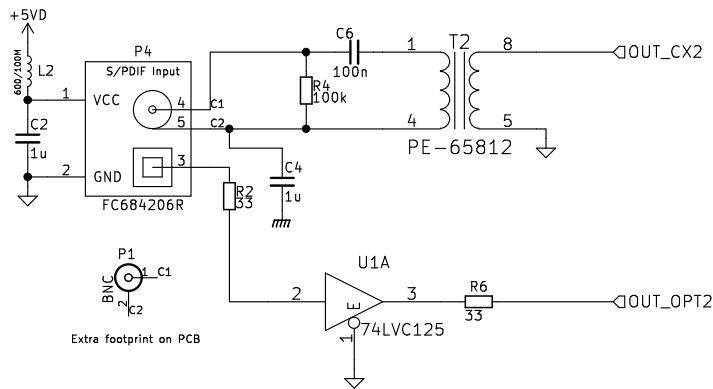
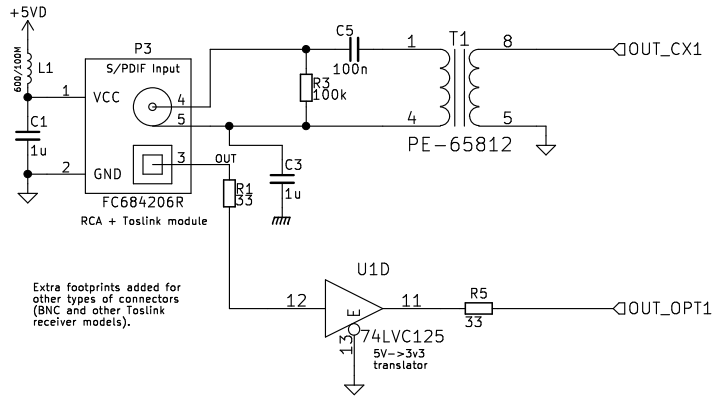
**Title: H-DAC**

Size: A4 Date: 2016-04-26  
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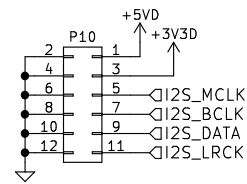
**Rev: v1.0A**  
Id: 1/5

# H-DAC v1.0A

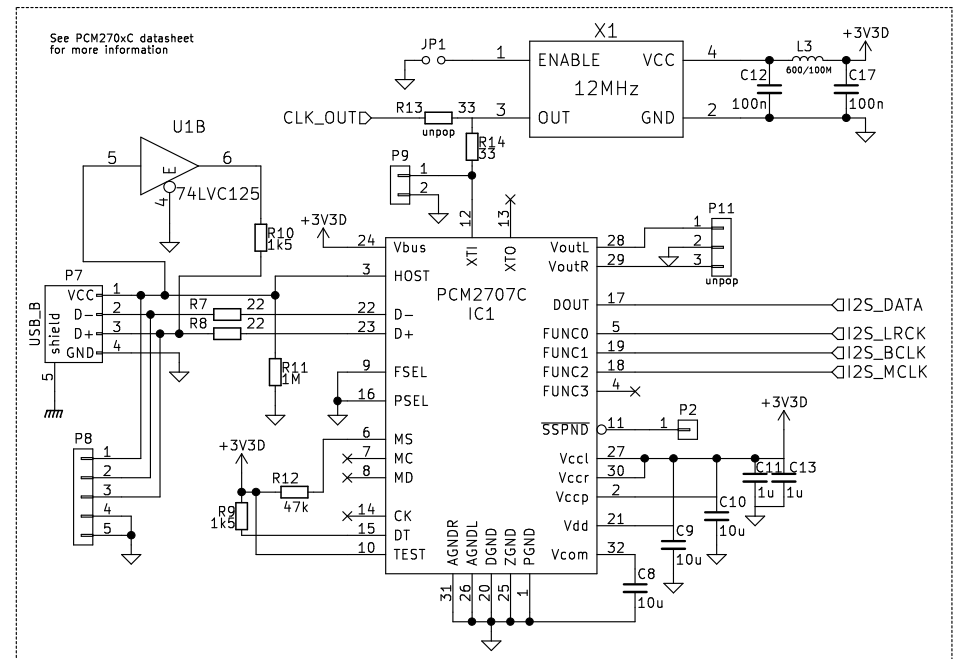
## Digital inputs



Inputs of U1D and U1A should also be connected to ground or 3v3 when not used.



Connector for external USB-I2S converter.



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Sheet: /Inputs/  
File: H-DAC\_v10A\_inputs.sch

**Title: H-DAC**

Size: A4 Date: 2016-04-26

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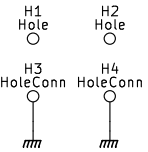
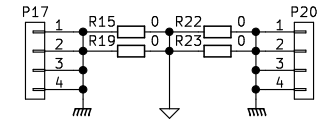
**Rev: v1.0A**

Id: 2/5

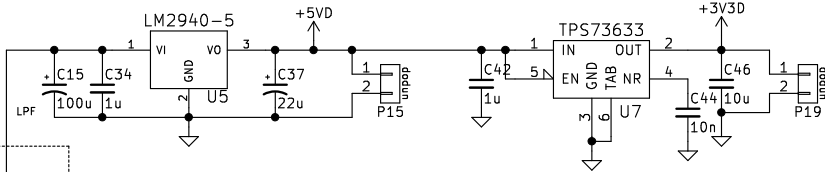
# H-DAC v1.0A

## Power Supply

Enclosure connectors, mounting holes, and enclosure ground connections (close to connectors).

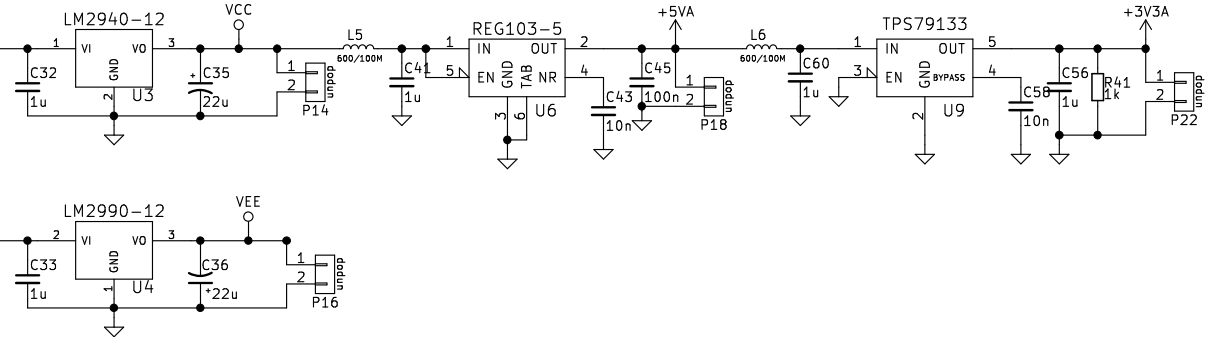


+5VD and +3V3D are digital supplies.



VCC and VEE are used for opamps.

+5VA is for DAC analog supply.



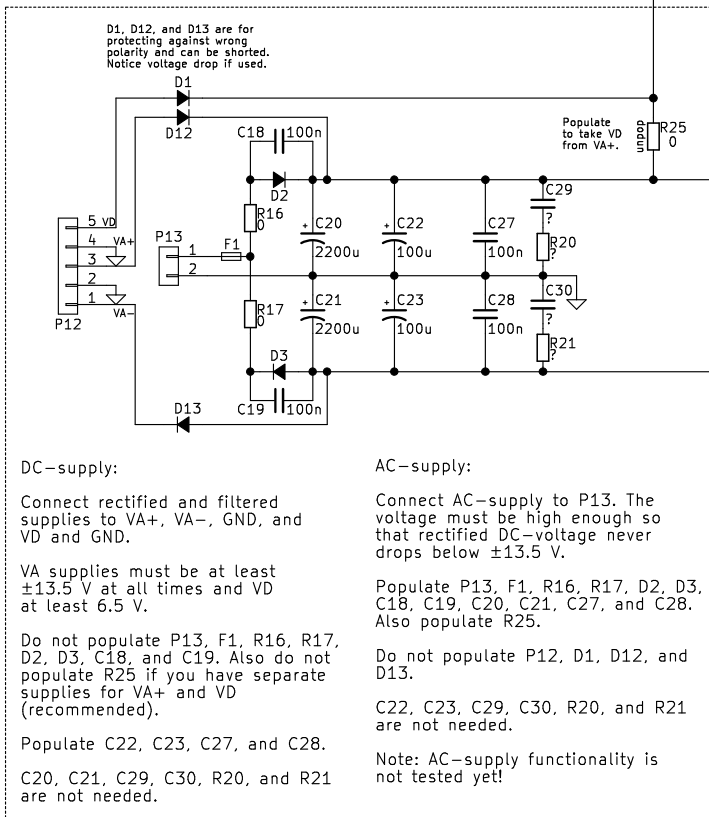
U5, U3, and U4 should be attached to heatsink or chassis.

C35, C36, and C37 should have ESR between 0.1 and 1 ohms.

Pinheaders P14, P15, P16, P18, P19, and P22 are for test purposes and can be omitted. External supplies can be connected to these instead of on-board regulators (in this case break ferrite links).

D1, D12, and D13 are for protecting against wrong polarity and can be shorted. Notice voltage drop if used.

Populate to take VD from VA+.



### DC-supply:

Connect rectified and filtered supplies to VA+, VA-, GND, and VD and GND.

VA supplies must be at least  $\pm 13.5$  V at all times and VD at least 6.5 V.

Do not populate P13, F1, R16, R17, D2, D3, C18, and C19. Also do not populate R25 if you have separate supplies for VA+ and VD (recommended).

Populate C22, C23, C27, and C28.

C20, C21, C29, C30, R20, and R21 are not needed.

### AC-supply:

Connect AC-supply to P13. The voltage must be high enough so that rectified DC-voltage never drops below  $\pm 13.5$  V.

Populate P13, F1, R16, R17, D2, D3, C18, C19, C20, C21, C27, and C28. Also populate R25.

Do not populate P12, D1, D12, and D13.

C22, C23, C29, C30, R20, and R21 are not needed.

Note: AC-supply functionality is not tested yet!

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Sheet: /PSU/

File: H-DAC\_v10A\_PSU.sch

**Title: H-DAC**

Size: A4 Date: 2016-04-26

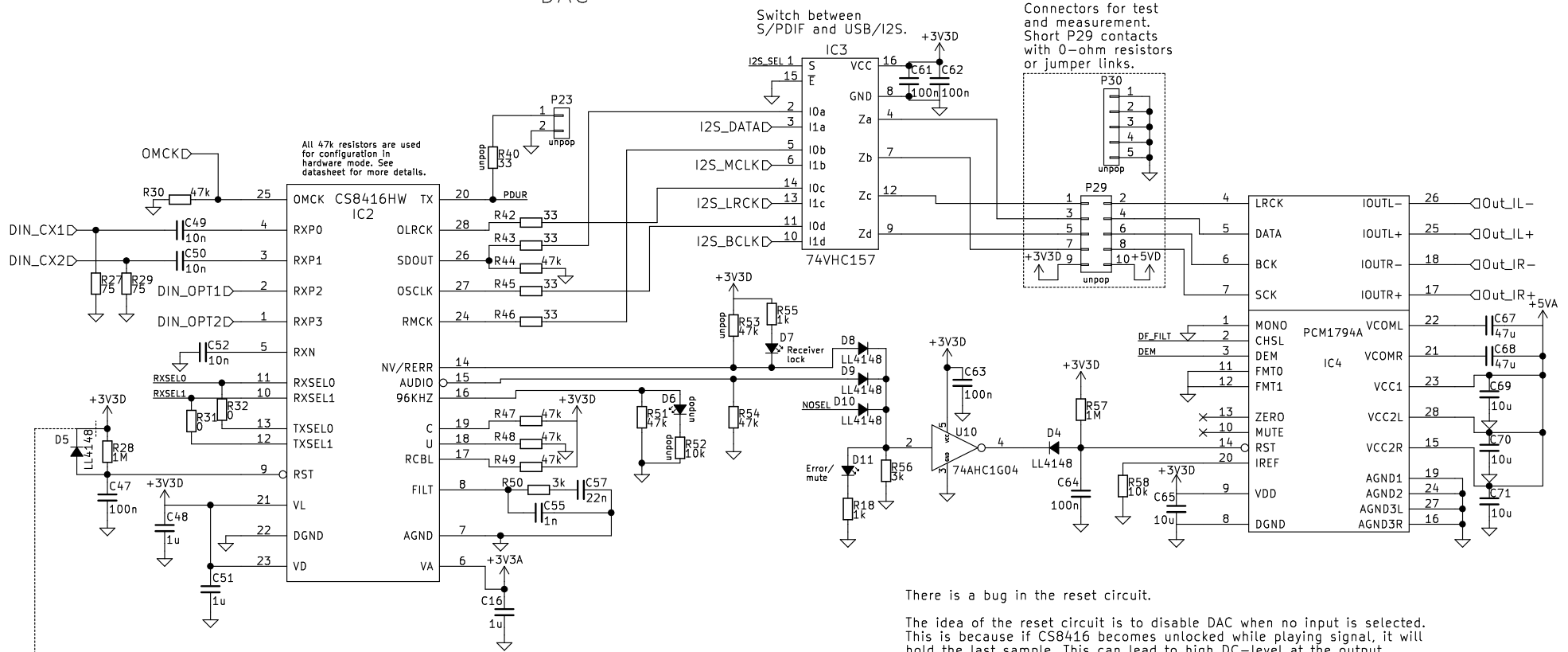
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**Rev: v1.0A**

Id: 3/5

# H-DAC v1.0A

## DAC



All 47k resistors are used for configuration in hardware mode. See datasheet for more details.

Switch between S/PDIF and USB/I2S.

Connectors for test and measurement. Short P29 contacts with 0-ohm resistors or jumper links.

Optional reset circuit fix. Works if DIN\_CX1 and DIN\_OPT1 are not used. Cut trace between D5 and R28/+3V3D, and connect D5 to RXSELO.

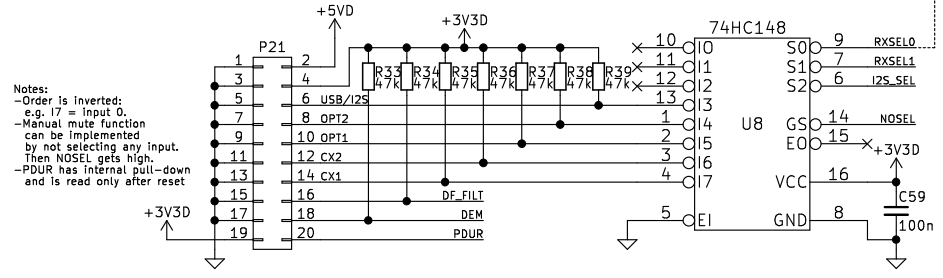
There is a bug in the reset circuit.

The idea of the reset circuit is to disable DAC when no input is selected. This is because if CS8416 becomes unlocked while playing signal, it will hold the last sample. This can lead to high DC-level at the output. However, the reset circuit does not work with USB/I2S.

Briefly:

- Use reset circuit as drawn if USB/I2S is not used.
- If Coax1 and Opt1 are not used (meaning using Coax2, Opt2 and USB/I2S), perform the mod shown with blue dotted line. In that case reset circuit works.
- Otherwise reset circuit cannot be used.

See nihtila.com for more information.

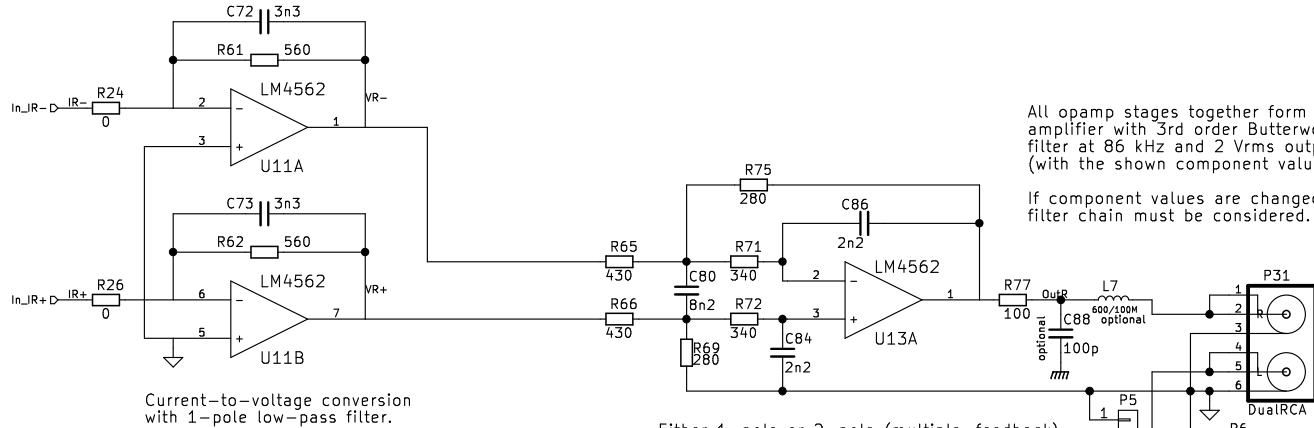


Notes:  
 -Order is inverted: e.g. 17 = input 0.  
 -Manual mute function can be implemented by not selecting any input. Then NOSEL gets high.  
 -PDUR has internal pull-down and is read only after reset

<b>Tomi Nihtilä</b>	
Sheet: /DAC/	
File: H-DAC_v10A_DAC.sch	
<b>Title: H-DAC</b>	
Size: A4	Date: 2016-04-26
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	Id: 4/5

# H-DAC v1.0A

## Analog stage

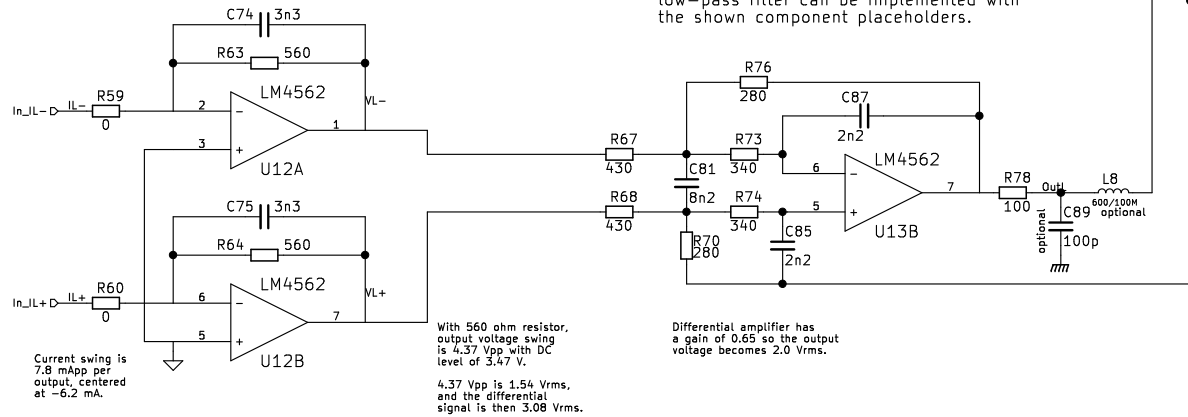


All opamp stages together form a transimpedance amplifier with 3rd order Butterworth low-pass filter at 86 kHz and 2 Vrms output level. (with the shown component values).

If component values are changed, the whole filter chain must be considered.

Current-to-voltage conversion with 1-pole low-pass filter.

Either 1-pole or 2-pole (multiple-feedback) low-pass filter can be implemented with the shown component placeholders.

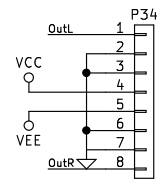
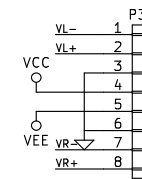
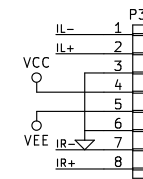


Current swing is 7.8 mApp per output, centered at -6.2 mA.

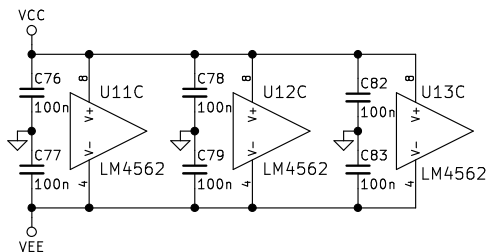
With 560 ohm resistor, output voltage swing is 4.37 Vpp with DC level of 3.47 V. 4.37 Vpp is 1.54 Vrms, and the differential signal is then 3.08 Vrms.

Differential amplifier has a gain of 0.65 so the output voltage becomes 2.0 Vrms.

Headers for addon boards. If no addon is used, do not populate.



Pins 2 and 7 are routed as signal returns and are not connected to GND plane.



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Sheet: /Analog stage/  
File: H-DAC\_v10A\_analog.sch

**Title: H-DAC**

Size: A4 Date: 2016-04-26

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**Rev: v1.0A**

Id: 5/5